April 1974 B74-10021

NASA TECH BRIEF

Goddard Space Flight Center

Data Processor With Conditionally Supplied Clock Signals

The problem:

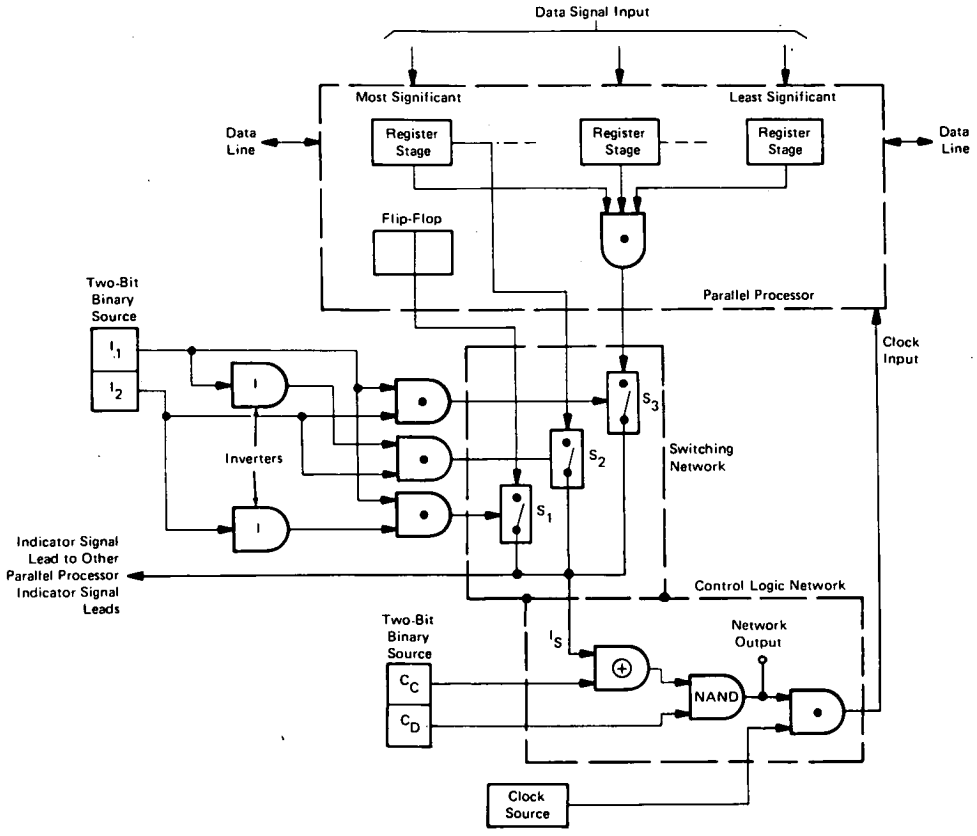
Most of the existing digital data processors use separate signal-carrying lines to control the application of clock pulses to the data storage registers. When large-scale integrated (LSI) networks are used, however, the separate signal lines become highly disadvantageous. These multiple lines result in fabrication problems and create an unnecessary space-and-power requirement for the integrated-circuit networks.

The solution:

In an improved, parallel data processor, clock pulses are conditionally supplied to the processing unit in response to the relative values of a binary bit of a control source and a binary bit derived on a single lead. Use of the single lead simplifies the fabrication of LSI networks.

How it's done:

The parallel processor (see figure) includes a number of separate register stages, each responsive to the



Parallel Processor

(continued overleaf)

respective data line. The least significant bit-register stage is selectively connected to the data line on the right, while the most significant bit-register stage is selectively connected to the data line on the left. These registers perform shift operations between each other in either direction and also rotate bits between the register stages in a right-hand direction to connect the least with the most significant stages.

The signals stored in the register stages can be added to or subtracted from the signals on the data lines. These signals can also be incremented or decremented in response to clock pulses applied to the processor. In addition, the processor can be activated so that each register stage is set simultaneously to a binary-one or to a binary-zero state. The signals on the data lines can be combined with those in register stages in accordance with the logical operations EXCLUSIVE OR, AND, and OR.

As shown in the figure, the two-bit binary word source can assume four two-bit combinations, i.e., binary 00, 01, 10, and 11. For combination 00, none of the indicator signals is fed from the processor through the switching network. For the combination 01, the state-of-overflow flip-flop is connected through switch S_1. For the 10, the negative indicating signal is fed from the processor through switch S_2. Finally, when the binary source supplies 11, outputs from all the register stages are fed through the AND gate and through switch S_3.

Three AND gates are provided for controlling the switches of the switching network, as shown. In addition, two inverters are provided at the output of the two-bit binary source.

The processor operates in response to the leading or positive-going edge of the clock pulse input which is controlled by another two-bit binary source and by the control logic circuit. The effect on clock pulses is shown in the following table:

Binary Source Signals		Indicator Signal I_S	Switching Network Output	Effect on Pulses From Control Logic
C_D	C_C			
0	0	0	1	Clock gated through control logic
0	0	1	1	Clock gated through control logic
0	1	0	1	Clock gated through control logic
0	1	1	1	Clock gated through control logic
1	0	0	1	Clock gated through control logic
1	0	1	0	Clock blocked by control logic
1	1	0	0	Clock blocked by control logic
1	1	1	1	Clock gated through control logic

When $C_D = 1$, it defines that a compare is to take place. C_C is then compared with I_S. Only if $I_S \neq C_C$ will the clock be inhibited. Therefore, the effect is to inhibit the parallel processor clock if the status or indicator test is false. For example an add if negative command can be defined. If $C_C = 1$, $I_S = 1$, $I_1 = 1$, and $I_2 = 0$, an addition will take place when Clock = 1. $I_S = 0$ will inhibit the clock and no addition takes place.

If on the other hand $I_1 = 0$ and $I_2 = 0$, this means that the I_S signal will come from another parallel process. The operation of the former processor depends on this processor. The next effect is now to add data to processor 1 if processor 2 is negative. Therefore, any processor can conditionally operate another processor.

The main feature of the entire system is a single lead that connects the switching network with the control logic circuit. A combination of this lead and the single lead that feeds the clock input into the processor makes the system easily adaptable to large-scale integration (LSI). As a result, this system allows a large number of circuit combinations.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
Goddard Space Flight Center
Code 207.1
Greenbelt, Maryland 20771
Reference: TSP74-10021

Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,702,463). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Goddard Space Flight Center
Code 204
Greenbelt, Maryland 20771

Source: Robert J. Lesniewski
Goddard Space Flight Center
(GSC-10975)